پوهنتون کاردان
KARDAN UNIVERSITY

Department of Information Technology

Faculty of Computer Science

Course Title:	Digital Logic and Design
Course Code:	**CS-105**
Coordinating Faculty/ Department	Faculty of **Computer Science/IT**
Credits:	04
Pre-requisite	***Introduction to IT***
Lecturer Name and Contact:	Mr. Wali Ullah Shinwari, 0093-782358093

General Course Information

- The coursework will consist of regular class activities to give students the basic concepts.
- This course introduces the basic principles and concepts of modern digital systems. This includes the study of combinational and sequential systems using standard modules such as shifters, adders, registers, and counters etc. The advanced techniques for designing, analysing and implementing the digital circuits are introduced with an emphasis on practical design techniques and circuit implementation. Major topics include number systems, Boolean algebra, logic components, combinational and sequential logic analysis and design, and digital subsystems. The laboratory provides more insight into the design and implementation of digital systems using the hardware components as well as programmable implementation technologies.

COURSE OBECTIVES

The objective of the course is to explain how digital circuit of large complexity can be built in a methodological way, starting from Boolean logic and applying a set of rigorous techniques. Numerous examples and case studies will be used to illustrate how the concepts presented in the lectures are applied in practice, and how the need to accommodate different practically-motivated trade-offs can lead to alternative implementations. The students will apply their knowledge in the labs by building increasingly more complex digital logic circuits. While Computer Organization and Microprocessors and Embedded Systems are listed in the calendar description, the primary objective of the course is not CPU design as such.

COURSE Learning Outcome

This course primarily contributes to the Computer Science program outcomes that develop student abilities to:

1. to apply knowledge of mathematics, science, and engineering.

2. to design and conduct experiments, as well as to analyze and interpret data.

3. to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

4. to identify, formulate, and solve engineering problems.

LEARNING REFERECNCES

1. M. Morris Mano& Michael D. Ciletti, Digital Design, 4th Edition, Pearson Prentice Hall, 2007.

2. Fundamentals of Digital Logic with Verilog Design, 3rd Edition

3. Introduction to Digital Systems by Mohammed Ferdjallah

TEACHING METHODS

1. Lecture:

Oral presentation by lecturer focuses on explaining topics, ideas and theories.

2. Conferences/ Discussion:

Two -way communication with and among the groups of students

3. Computer Based practices:

Network computer labs

4. **SIMULATIONS**

Class Room Etiquette:

Class room courtesy is expected of all students all the time. Following is general guidelines for the class room conduct:

1. Refrain from chatting with fellow students.
2. Arrive on time. If you come late please be courteous to other students
3. Do not get up and walk out halfway through class.
4. Do not cut the instructor off at the end of class.
5. All cell phones and pagers must be turned off during class and examination.
6. Eating is not permitted.
7. Above all please be cognizant of the learning process and purpose of you being in the class room and extend same respect to other students.

POLICIES & GUIDELINES

Guidelines for Format of Assignments: (General Recommendations)

1. attendance & Absences – Students are expected to attend and sit through the entire class meetings. In case of an absence, the student is responsible to arrange for notes and missed announcements.

2. Assignment Completion & Late Work – Late assignment submission is not allowed unless permission is granted by the instructor prior to the deadline. Students should submit their assignments in the LMS by the due date, other sources of submission for the assignments are not allowed.
3. Academic Conduct Code – Cheating and plagiarism will not be tolerated in any case. They will result in no credit for the assignment or examination and may lead to disciplinary actions.

Course Schedule / Contents

Week No.	Topics for Discussion	Book Chapter #	Suggested Activity	Topic Outcomes
1	**Introductory**	First	The course will be introduced. In the introduction explain that what we will study in the course and how this course is helpful for students in future studies for designing Circuit.	A Complete detail about all topics and finally whole subject.
2	Number systems, Number systems conversions, decimal to binary and vice versa, decimal to octal and vice versa, decimal to hexa decimal and vice versa. Some other conversions. Binary Addition, Subtraction , Multiplication and Division	First	Conversion from Binary to Decimal and vice versa After familiarizing with the basics of binary numbers, next students will be given problems to solve related to addition, subtraction , multiplication and division	1. Deep knowledge of various number systems suitable for representing information in digital systems. 2. Mathematical Operations of different Number System.
3	Concept of Signed Numbers and Unsigned Numbers 2's Complement Form Range of Binary Numbers, Memory location and its range	First	Students will be given problems to solve related to 2's complement form. Pre-test and Post-test and Summarizing techniques will also use.	.The major Concept of subtraction for two numbers by the adder circuit. .

	for signed, unsigned etc.			
4	BCD encoding scheme, ASCII, EBCDIC, UTF-8, UTF-16 & UTF-32 Alphanumeric Code	First	Class assignment will be given to the students to explain the role of different codes.	1. Concept of BCD and Mathematical operations of BCD. 2. Understand how computer assign binary codes to different languages letters.
5	Error detection in transmission: Parity checking Longitudinal Redundancy check, checksum & cylic redundancy check method			
6	Logic Gates Basic Building Blocks Logic Gate Symbols, expression, truth tables, circuits	Second	Feedback on paper for understanding the Concept of Logic Gates	1.Concept Logic Gates 2. Importance and usage of the Five Logic Gates
7	Truth or Function Table Function or Boolean Expressions Timing Diagram	Second	Making of 3-variableTruthtable pre-test and post-tests and summarizing techniques will also use..	.Making Truth table and Timing diagram of each logic gate and its importance
8	Combinational Circuit, circuit drawing from Boolean expression and vice versa.	Three	Some expression will be given for design of Circuit. pre-test and post-test technique as evaluation..	Designing of Combinational Circuit from the Expression.
9	Introduction to Boolean Algebra and Logic	Three	Feedback of the explained topic	Basic postulates of Boolean algebra and shows the correlation

			on paper.	Between Boolean expressions and their corresponding logic diagrams.
10	Description & Analysis of various Logic gates , axioms, laws and simplifications.	Four	Practice of Making Combinational circuit. pre-test and post-test and summarizing techniques will also use.	All possible logic operations for two variables are investigate and the most useful logic gates used in the design of digital systems are identified.
11	commutative, associative, distributive Laws and Rules in Boolean algebra Drawing of Simplified Circuits.	Five	Different expressions are given for simplification.	Simplification of Combinational circuit by Rules and Laws
12	Circuits drawing from Boolean function, Deriving Boolean expressions from functions, Evaluation of Boolean expressions	Six	All the expressions have been simplified by laws, axioms. Circuits will be drawn and expression will be evaluated. Karnaugh map will be discussed.	Circuits understanding and manipulation and drawing and then systematic method.
13	Seven-Segment Display	Seven	Designing Combinational circuit for different edges of Seven Segment display.	Designing of combinational circuit for 7-Segment.
14	Designing of different Combinational circuit	Eight	Design Circuit for different combinational circuits.	Half, full. N-bit adders
15	ADDERS, Subtractor	Eight	Full-adder circuit designing. pre-test and post-test and summarizing techniques will also use.	Designing of Half and Full Subtractor Circuits
16	Sequential Circuits, registers		D-Latch, Circuit designing	Designing of

		Nine	of Shift Register	1. RS Latch 2.D Latch Basic types of registers

COURSE ASSESSMENT

TYPE	PERCENTAGE	RATIONALE
Internal Assessment - Assignments: 10% - Quizzes: 10% - Attendance: 5%	25 %	Equal weightage is assignments and quizzes and at the same time emphasizing on the importance of class participation.
External Assessment - Midterm: 25% - Terminal: 50%	75%	Students develop an examination sense through midterm examination hence 25% weightage is appropriate. Midterm duly followed by terminal examination providing 50% weightage which is an opportunity to improve scores appropriately.

GRADING

MARK RANGE	GRADE POINT	GRADE	EXPECTED RESULT
90 and above	4.0	A	At least 15% expected to secure A grade
80 – 89	3.0	B	At least 25% expected to secure B grade
70 – 79	2.0	C	At least 25% expected to secure C grade
60 – 69	1.0	D	At least 30% expected to secure D grade
59 and below	0.0	F	At least 5% expected to secure F grade

Kardan University Policy on Plagiarism:

All examinations and quizzes will be "closed book" unless otherwise instructed. At the time of examination all students are requested to clear their desks and are not allowed exchanging any notes or electronic (text) messages to other students. All cellular phones should be in silent mode and student will not be allowed to use it during the examination other than medical/family/work emergency. All students are expected to adhere to these policies and procedures.

Conduct and Important Policies:

Any student found guilty of a breach of ethics will be referred to Disciplinary Committee of the University.

a) Breach of ethics includes, but is not limited to plagiarism (the copying of other's ideas and passing them off as one's own); copying or other forms of cheating on examinations, papers, and reports; the sale, purchase, or distribution of term papers It is within an instructor's discretion to impose a lesser penalty, e.g., "zero" grade on a given assignment.

b) Course registration is charged by the management. Please approach the management for any queries about course enrolment. In no circumstances should you approach the lecturers who have no control on this.

c) Make-up exam for midterm and terminal exam is available only for those individuals, who are not able to attend their regular exams. Provision of supported documents are mandatory for grant of approval to participate in make-up exams. Those students who miss their regular exam without a genuine reason, will be entitled for 80% of total makeup marks.

Usually make-up exam starts a week after the regular exam finishes.

d) There is no make-up session for the oral presentations and quizzes. If you are absent from the oral presentation/ quiz without eligible reasons/documents, you will not earn any marks.

e) All examinations and quizzes will be "closed book" unless otherwise instructed. At the time of examination all students are requested to clear their desks and are not allowed exchanging any notes or electronic (text) messages to other students. All cellular phones should be in silent mode and student will not be allowed to use it during the examination other than medical/family/work emergency. All students are expected to adhere to these policies and procedures.

f) There is no supplementary exam for any failed course. Individuals, who fail the course, must retake the module.

Attendance:

Your regular and punctual attendance at lectures and seminars is expected in this course.

University regulations indicate that if students attend less than 65% of scheduled classes, they may be refused from final assessment.

This course policy has been approved in the Curriculum Development Committee meeting FCS/CDC-2025-04.

Head of Committee Signature.....

Dean, Faculty of Computer Science Signature .....